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Shunt Active Power Harmonics Filter Performance Evaluation for ASD applications

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Abstract
In this paper the performance evaluation of a three-phase Shunt Active Power Filter (SAPF) for harmonic mitigation in power systems with common Adjustable Speed Drives (ASDs) systems are presented. The application is modeled and simulated under different operating conditions. The system is mainly assessed in terms of line current THD_i, total power factor TPF, unbalance supply sensitivity, dynamic response, and DC-link voltage regulation. Originally contributed is the study of key controller's parameters effect. The success of the study reveals the trade-off relation of controller's constraints & system performance with the SAPF cost reduction possibilities.

Keywords: ASD, Active filter, Harmonics, Controllers, Cost reduction, THD.

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تقييم مرشح توافقيات القدرة المتوازي لتطبيقات قيادة محركات متعددة السرعات

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الملخص

تتناول هذه الدراسة تحليل وتقييم استراتيجيات التحكم الخاصة بمرشح القدرة الفعال المتوازي ثلاثي الطور (Shunt Active Power Filter – SAPF) المستخدم للحد من توافقيات تشوه التيار الكهربائي وتحسين جودة القدرة الكهربائية في أنظمة قيادة المحركات ذات السرعات المتغيرة (Adjustable Speed Drives – ASDs) الشائعة صناعيا لمزاياها المعروفة وقدرتها الفائقة على التحكم وتوفير الطاقة المستهلكة. تم نمذجة ومحاكاة النظام باستخدام برنامج MATLAB \ Simulink تحت ظروف تشغيل مختلفة من خلال عدة مؤشرات أداء، أهمها التشوه التوافقي الكلي للتيار(THDi) ، ومعامل القدرة الكامل (TPF)، والاستجابة الديناميكية وتنظيم جهد ناقل التيار المستمر. يتمثل نجاح الدراسة في المساهمة لكشف تفاصيل فجوة تحديد علاقة التوازن بين مؤشرات الأداء ومعايير نظام التحكم المستخدمة الرئيسية Proportional–Resonant Controller – P–Q Control & DC Bus Voltage Regulation وكذلك بيان حالات إمكانية تخفيض تكلفة نظام المرشح SAPF طبقا للمعايير المطلوبة من مؤشر ضبط مستويات التحكم لتوافقيات التشوه في منظومات الطاقة الكهربائية حسب آخر تحديث IEEE 519–2022.

الكلمات المفتاحية: المحركات ذات السرعة المتغيرة – المرشح ألفعال – التوافقيات – المحكمات – تخفيض التكلفة – التشوه التوافقي الكلي.

1- Introduction

Adjustable speed drives (ASDs) are widely used in industrial applications due to their well-known benefits 2026 [1], [2], [3].

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Most ASD systems use a six-pulse rectifier which draws distorted current characteristics into the power system [4],[5]. Typically, these currents contain dominant 5th, 7th, 11th, and 13th harmonic components 2020 [6]. They increase current distortion, reduce power factor (P.F.), cause additional losses and may lead to voltage distortion at the Point of Common Coupling (PCC). Consequently, harmonic mitigation is required to satisfy power quality standards such as IEEE 519-2022 [7]. Active Power Filters (APFs), unlike passive filters, utilize power electronic converters and control algorithms to actively compensate harmonic distortion. They operate by generating compensating currents that counteract unwanted harmonic components. The paper contribution involves the performance evaluation of a SAPF-ASD system under different operating conditions and diverse controller parameters variation. Unbalance supply voltages, loading factor variation along with controller cutoff frequency & gains deviation are implemented and assessed. Transient DC voltage overshoot & rise time analysis along with attempting SAPF technique cost reduction can be considered as original achievement of this study.

2- SAPF Utilized Simulation Model Description:

The overall configuration of the SAPF-ASD system is developed based on a recent realistic hardware-oriented configuration derived from the TPI8032 converter platform 2025 [8] . The modeling approach includes both the power and the control stages, ensuring accurate representation of electrical dynamics, switching behavior, and closed-loop control interactions. The main components and control structure of the SAPF are described subsequently.

3- SAPF Operation & Control Description:

The SAPF model used in this study is based on the reference technical implementation reported in [8], including both the power stage and control system. The model reveals system dynamics and switching behavior that facilitates the study objectives. It involves the AC-side subsystem, Voltage Source Inverters (VSI), DC-link, and utilized controllers such as Phase-Locked Loop (PLL), Instantaneous Reactive Power (P-Q) theory, Proportional Resonant

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(PR) controller, and DC-link voltage regulation. System block diagrams, operation stages & sequence details flowchart are presented & fully described in the related B.Sc. study 2026 [9]. Briefly, it outlines the sequence of measurement, synchronization, reference generation, control, and switching processes used to achieve harmonic compensation and DC bus voltage regulation. Initially, the control process begins with SAPF system initialization and measurement of grid signals, followed by synchronization using the PLL controller. Measured quantities are transformed into the d-q reference frame for power calculation and harmonic extraction. Based on the DC bus voltage condition, a typical Proportional Integral (PI) controller is activated to generate the loss component. The reference currents are then transformed back to the abc frame and tracked using a current controller. Finally, PWM signals are generated to control the inverter, enabling the SAPF to inject the necessary compensating currents and maintain continuous operation. The following sections briefly describe the Simulink models used in the well-known & common defined theories.

3.1- SAPF Closed-Loop Control System: To achieve effective harmonic mitigation, the SAPF control system is capable of detecting harmonic components and generating compensating currents in real time. The implemented closed loop control architecture, shown in Fig. 1, includes coordinated subsystems responsible for grid synchronization, reference current generation & regulation, and DC-link voltage stabilization.

The SAPF closed loop control system includes the following subsystems:

(a) Grid synchronization using a Phase-Locked Loop (PLL): This subsystem controller is used to estimate the grid phase angle and frequency required for synchronization and control implementation.

(b) Reference current generation using P–Q theory: The instantaneous power P–Q well known theory is applied to extract harmonic components and generate the reference compensating currents. The instantaneous P and Q powers can be expressed as the

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sum of their average and oscillating components. Then the reference currents must be derived from the calculated power components. Full details are presented in the B.Sc. related study [9].

(c) Current control using PR controllers: Proportional–Resonant (PR) controller subsystem is used to regulate the compensating current injected by the SAPF. The PR enables accurate tracking of sinusoidal current references minimizing the steady-state error 2021 [10].

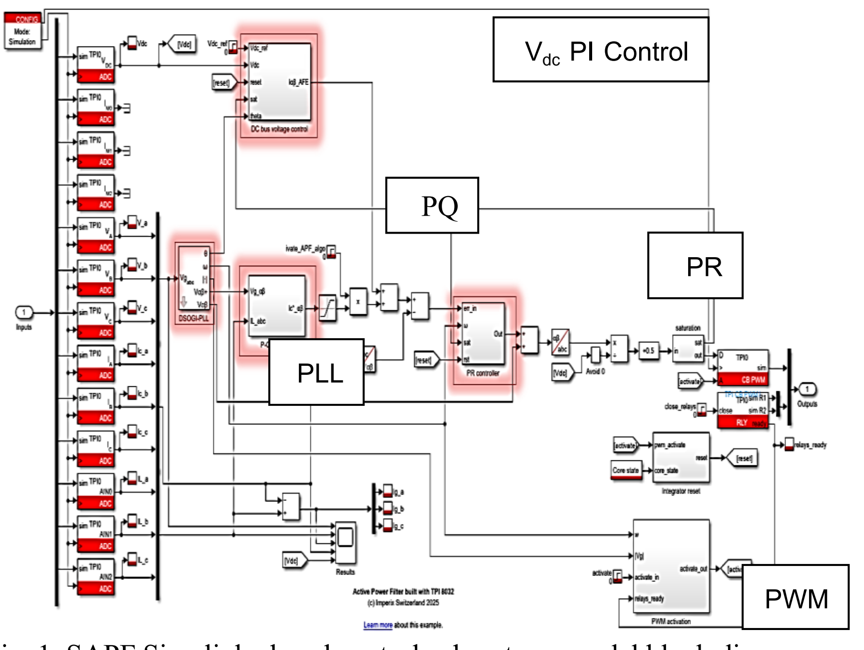

Fig. 1. SAPF Simulink closed control subsystems model block diagrams.

The transfer function of the PR controller is given by:

$$G_{PR}(s) = K_p + \frac{2K_i\omega_c s}{s^2+2\omega_c s+\omega_0^2} \quad (1)$$

where K_p & K_i are the proportional and resonant gains at the selected harmonic, the ω_c is the cutoff frequency variable determining the bandwidth around the resonant peak & ω_o is fundamental resonant frequency.

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(d) DC-link voltage control using a PI controller: The PI controller regulates the DC-link voltage at assigned value to ensure stable SAPF operation. The DC-link capacitor serves as an energy storage element, providing the energy required during transient and compensation processes while maintaining the inverter voltage level. The control process begins by comparing the measured DC bus voltage with the reference voltage. The error signal is defined as the difference between them.

(e) SAPF (DC&AC) sides power stage model: This represents the interface between the grid and the load. It is connected in parallel at PCC and includes the DC side subsystems, VSI, and the AC side subsystems. The DC side subsystem consists of the DC-link and the DC electromagnetic compatibility (EMC) filter. The EMC filter is used to suppress high-frequency switching noise and improves the overall system stability. The DC bus parameters, used for voltage regulation within the closed-loop control system, are presented in Table 1. Maintaining a constant DC-link voltage is essential for proper operation, as the compensating current depends on the available DC voltage. AC&DC power stages models are fully detailed in [9].

Table 1 DC Bus Simulink SAPF Model Parameters [8]

Parameter	Value
Initial DC bus voltage (V_{dc0})	650 V
DC bus capacitor (C_{dc})	1.5 mf
DC bus reference ($V_{dc.ref}$)	800 V

The AC-side subsystem enables controlled current injection into the grid and ensures electromagnetic compatibility. It consists of a three-phase grid model, grid impedance, nonlinear load, AC-Side EMC filter, AC-Side Pre-charge Circuit for DC-Link Capacitor. The electrical parameters of the utility grid model used in the SAPF-ASD system simulation, including grid voltage, frequency, and line impedance elements are presented in Table 2.

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Table 2 AC Side Simulink SAPF Model Parameters [8]

Parameter	Value
Grid Phase Voltage (RMS)	230 V
Grid Frequency (f)	50 Hz
Main inductance (L_g)	1.05 mH
Series resistance (R_g)	54 $m\Omega$

4- SAPF Simulation Results & Performance Evaluation:

4.1- Simulation at Rated Operating Point of the SAPF-ASD System

This preliminary results section presents the baseline performance of the SAPF under nominal operating conditions. The system performance is initially evaluated at the rated load with balanced grid voltage to verify proper operation before applying disturbances or parameter variations. Fig. 2 shows the line current waveform and its corresponding FFT spectrum for the ASD rectifier load before compensation.

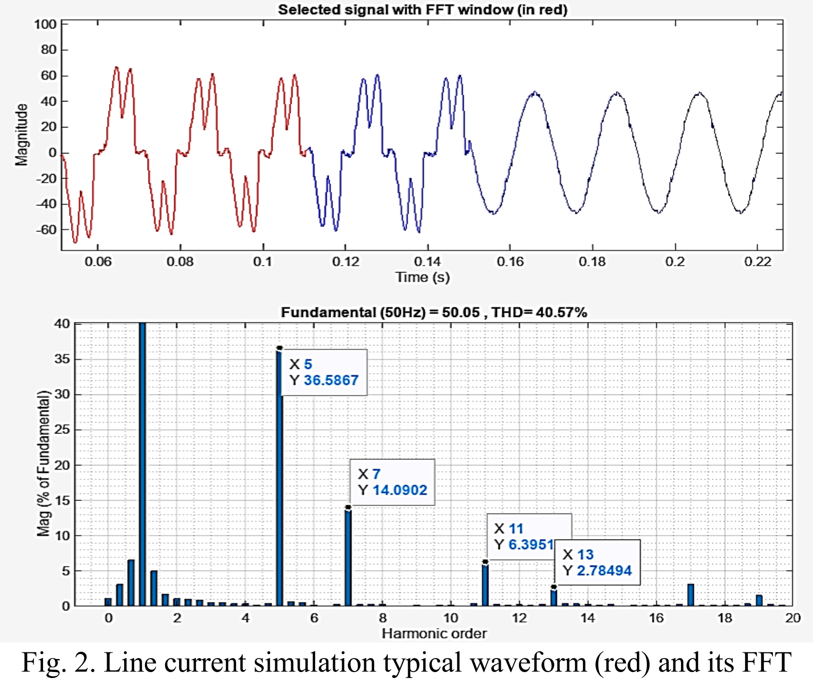

Fig. 2. Line current simulation typical waveform (red) and its FFT spectrum with 41% THDi of an ASD system.

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As observed, the line current waveform (first 3 red cycles) is highly distorted with 41% THDi. Fig. 3 presents the line current waveform (3 red cycles) after the implementation of the SAPF @ 0.15 sec & FFT spectrum. The filter injected compensating currents effectively eliminating the dominant harmonics resulting in 4.58% line current THD_I value satisfying the IEEE 519-2022 harmonic minimum constricted limits [7].

Full comparison with other passive, hybrid filtering options have been presented in [8] confirming the superiority of SAPF systems on the expenses of cost consideration that has been also successfully reduced in this piece of work (shown in Table 9).

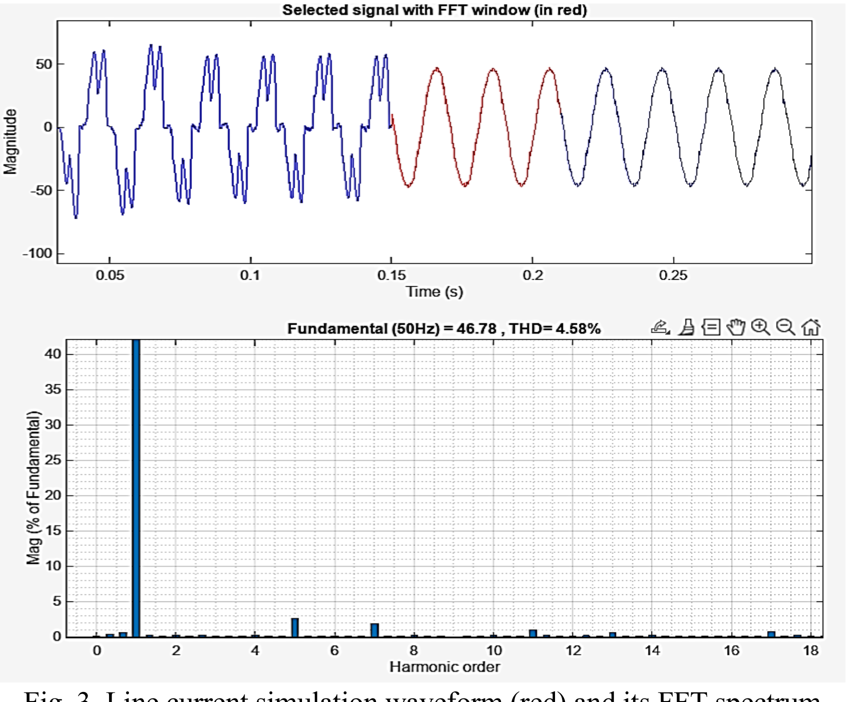

Fig. 3. Line current simulation waveform (red) and its FFT spectrum after SAPF compensation with 4.58% THDi (22kW).

4.2- P–Q Control Strategy Testing Analysis:

Load Variation Sensitivity: To evaluate the SAPF performance under different operating conditions, the SAPF–ASD system is

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tested at three different loading levels along with balanced and unbalanced supply voltage conditions. This involves the full load, half load and light load cases of 22 kW, 11 kW, 5.5 kW power ratings, respectively.

a) **Balanced Supply Voltage Conditions:** Fig. 3 showed already the Line current after the SAPF compensation at full load (22 kW) with THDi value reduced to approximately 4.58%, and comply with the harmonic limits recommended by IEEE 519-2022 [7]. Table 3 presents all described results and conditions. All waveforms are presented in the related B.Sc. study [9].

Table 3. TPF & THDi performance of the grid current before and after SAPF compensation under different loading conditions.

Level	$R_{dc}(\Omega)$	TPF w/o SAPF	TPF with SAPF	THDi%	TDD%
Full load	12.5	0.895	0.968	4.58	4.58
Half load	25.0	0.879	0.954	7.24	5.30
Light load	50.0	0.875	0.950	***11.90***	4.33

b) **Unbalanced Voltage Conditions:** Common voltage unbalance levels up to 3% are introduced to evaluate the performance of the SAPF-ASD system, according to the NEMA standard 2020 [11]. As shown in Table 4, the THD of the grid current increases due to the voltage unbalance under all three loading conditions considered. The shaded two TDD conditions do not comply with the regulations of a less than 8.0% range.

Table 4 Grid current TDD under different voltage unbalances & load conditions

Voltage Unbalance	TDD%@22KW	TDD%@11KW	TDD%@ 5.5KW
0 (%)	4.58	5.30	4.33
1 (%)	4.96	5.46	4.93
2 (%)	6.37	7.59	5.99
3 (%)	***8.12***	***8.93***	7.33

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4.3- PR Controller Testing Analysis: The objective is to assess controller key parameter variation sensitivity and effects on harmonic mitigation capability and system dynamics.

a) Cutoff Frequency (ω_c) Variation: Low, nominal & high cutoff frequency cases were considered. As shown in the Table 5, while low ($0.1\omega_c$) enhance most of the performance parameters, high ($10\omega_c$) value has a contrary effect on most of the parameters as highlighted (***bold & italic***) in the table.

b) Integral Gain (Ki) Variation: Table 6 illustrates the effect of similar Ki value variation cases on several performance parameters, related to controller mission of regulating compensating current injected by the SAPF. As ***slow & weak*** indicators may appear at low Ki gain values, similar concerns may also exist of different parameters at high Ki gain values, as emphasized.

Table 5 Qualitative analysis of PR controller performance under different cutoff frequency (ω_c) conditions for each harmonic

Performance	($0.1\ \omega_c$)	Nominal ω_c	($10\omega_c$)
Response Speed	***Slow***	Balanced	Fast
Stability Margin	High	Adequate	***Reduced***
Frequency Selectivity	High	Moderate	***Reduced***
Noise Immunity	High	Acceptable	Low
Tracking Ability	High	Good	***Reduced***
Overall	Stable	Optimal	Fast & less ***robust***

Table 6 PR controller performance under different integral K_i gain

Performance	($0.1K_i$)	Nominal (K_i)	($10K_i$)
Dynamic response	***Slow***	Balanced	Fast
Harmonic tracking ability	***Weak***	Good	Very strong
Stability margin	High	Moderate	***Low***
Noise sensitivity	Low	Moderate	***High***
Overall	Sufficient	Optimal	***Risky***

C) DC Bus Voltage Control: The performance is evaluated by varying both PI gains (K_p, K_i) and the frequency bandwidth

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controller (ω_c), individually. Their effects on voltage regulation, response speed, and harmonic performance are numerically analyzed.

i) PI Gain Variation (K_p, K_i)**:** similarly, the overall performance comparison under different three (low, nominal, high) PI gain conditions is summarized in Table 7. Noticeably, the low gain case, has a Vdc ripple of 6.5% that exceeds the acceptable range (<5) 2026 [12], while high gain case has tripled the line current THDi to around 15%.

Table 7 Performance comparison of the SAPF-ASD system under different PI controller Kp, Ki gain assigned conditions.

Performance	Low Gains ($0.1K_p$,$0.1K_i$)	Nominal Gains (K_p,K_i)	High Gains ($10K_p$,$10K_i$)
Transient Rise Time	91 (ms)	24 (ms)	23 (ms)
Transient V_{dc} Overshoot	4.75 %	0.75 %	0.625 %
Line current THD_I (%)	4.96 %	4.58 %	***14.94 %***
V_{dc} ripple% @S.S.	***6.5 %***	2%	1.375%
Overall	Very stable	Balanced	***Risky***

ii) Frequency Controller Bandwidth (ω_c): Table 8 reveals, as indicated, a 26% reduction in transient rise time at 50 Hz. Moreover, the transient V_{dc} overshoot is also significantly reduced at higher frequencies to 0.75%. Comparing results to the nominal bandwidth condition (25Hz) indicate that, unlike the PI gain (K_p, K_i) variation cases, frequency variation does not significantly impact the harmonic performance of the SAPF-ASD system.

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Table 8 Performance comparison of DC bus voltage regulation under different controller bandwidth frequency conditions

Performance	Bandwidth variation		
	10 Hz		10 Hz
Transient Rise time	31.0(ms)	Transient Rise time	31.0(ms)
Transient V_{dc} Overshoot	2.63%	Transient V_{dc} Overshoot	2.63%
Line current THD_I	4.66%	Line current THD_I	4.66%

4.4- Targeted Harmonics Mitigation Cases: Cost-wise point of view, a simplified analysis was conducted. Full harmonics compensation case was considered as reference scenario & inverter market cost [12]. Table 9, noticeably, shows that one-third (33%) of the filter inverter cost can be saved in a flexible IEEE519 harmonic distortion assigned levels (<20%) for ISC/IL > 1000 condition in Case A. Meanwhile, case B provides 12% less cost [7].

Table 9 Performance comparison of harmonic compensation under different dominant harmonic scenarios SAPF-ASD system (22KW)

	Harmonics targeted	THD_I %	THD_I reduction %	Cost ($)	Cost Reduction
A	5^{th}	***16.5***	-24.5%	13,080	32.4%
B	5^{th},7^{th}	***9.07***	-31.93%	17,060	11.9%
C	5^{th},7^{th},11^{th}	5.19	-35.81%	19,130	1.2%
D	5^{th},7^{th},11^{th},13^{th}	4.58	-36.42%	19,360	0.0 (base)

5- CONCLUSIONS

In this work the assessment of a three-phase SAPF method for harmonic mitigation of ASDs has been studied. The SAPF reduced the line current THDi under nominal operating conditions meeting power quality standards with minimum sensitivity to load variations & supply unbalance. The influence of the controller main parameters variations has been originally investigated &

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contributed. Results reveal the trade-off behavior of the system performance to both PR controller parameter variations. Similarly, while increasing PI controller gains improved the damping capability at the cost of greater THDi, reducing the gains improved system stability at the expense of higher Vdc ripple%. Finally, the DC-link voltage controller effectively regulated V_{dc} at the assigned value with negligible sensitivity to bandwidth frequency variation. Outstandingly, considerable cost reduction of SAPF technique has been achieved for flexible IEEE519 line currents THDi requirements. Overall, the study aids in selecting proper system controller's parameters, complying with harmonics regulations along with cost reduction capability achievement. The study can be extended to similar rectifiers front end wide application.

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